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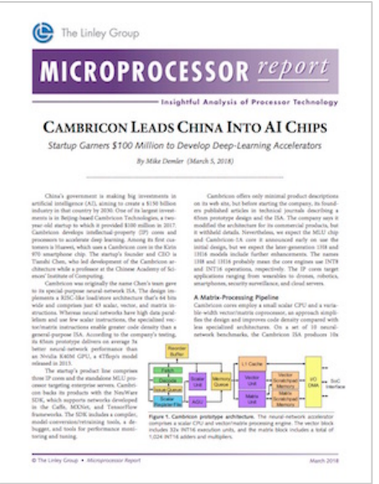
Roadmap Directions for the RISC-V Architecture

Andes RISC-V Con
November 13, 2018

Linley Gwennap, Principal Analyst

About Linley Gwennap

- Founder, principal analyst, The Linley Group
  - Leading vendor of technical reports on semiconductor products
- Editor-in-chief of *Microprocessor Report*
  - MPR is the leading microprocessor-industry newsletter for 30+ years
  - Linley has written recent articles on AMD, Arm, Graphcore, Huawei, Intel, Marvell, MediaTek, Nvidia, NXP, Qualcomm, Samsung, et al
- Coauthor of "A Guide to Processors for Deep Learning"
- Former CPU designer at Hewlett-Packard


The Linley Group
MICROPROCESSOR report
Insightful Analysis of Processor Technology
CAMBRICON LEADS CHINA INTO AI CHIPS
Startup Garners $100 Million to Develop Deep-Learning Accelerators
By Mike Demler (March 5, 2018)

Agenda

- RISC-V progress
- RISC-V roadmap
- Taking on ARM
- RISC-V challenges

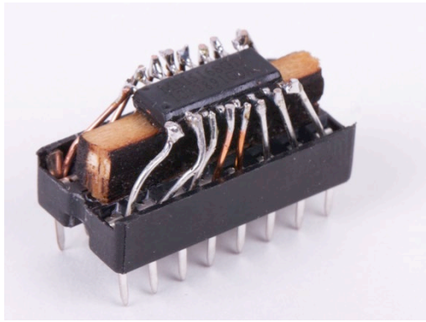
RISC-V Offers Disruptive Business Model

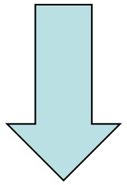
- Open-source instruction set created at UC Berkeley
  - Full instruction set for building general-purpose CPUs
    - Specialized features (e.g. DSP, vector extensions) still in development
  - Anyone can use with no license fees
  - Anyone can add custom instructions for special functions
  - Software ecosystem is developing
- Open-source CPU cores also available
  - No license fees for these cores
  - Users can modify or extend the RTL to meet their needs
  - But open-source cores may lack commercial features, validation, and support

Large Chip Vendors Replace In-House ISAs

- Significant interest from Nvidia, AMD, HP, Qualcomm, etc
- These companies have developed small proprietary CPU designs
  - Often used for power management, configuration, testing, and similar tasks
  - Often embedded inside larger processor chips or SoCs
  - Often use proprietary instruction sets with in-house development tools
  - Easy to port small in-house software stack
    - No need to run customer code or third-party applications
- Converting these designs to RISC-V simplifies software development
  - Leverage open-source and third-party tools
- Nvidia has publicly committed to this approach for its GPUs

In-house kludge





RISC-V

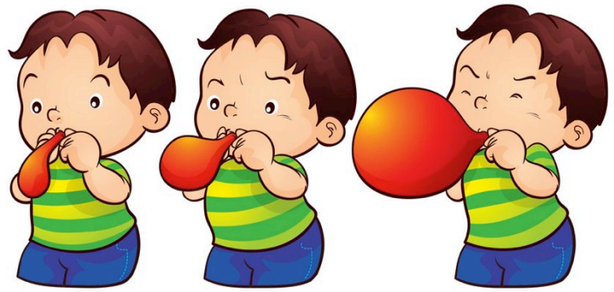
Chip Startups Adopt, Modify RISC-V

- Abee uses RISC-V in a low-power processor for wearables
  - Huami launched smartwatch and fitness band using RISC-V
- Esperanto is designing an AI accelerator using two custom RISC-V CPU designs (Maxion and Minion)
- Greenwaves is sampling an MCU with integrated AI engine using RISC-V for both the main CPU and the accelerator
- Mythic is developing an AI chip that combines analog computation with a set of small RISC-V cores
- These companies often modify or extend the RISC-V instruction set to optimize performance on target application (e.g. AI)

CPU IP Vendors Adopt, Support RISC-V

- Andes is an established CPU IP vendor that has adopted RISC-V
  - Andes developed its own ISA and licensed into >2.5 billion chips
  - It now offers CPUs that implement basic RISC-V ISA plus custom extensions
- Cortus has taken a similar approach
- These CPU vendors benefit from larger RISC-V ecosystem
- SiFive, Incore, Syntacore, other new IP vendors also license RISC-V CPUs
- Microsemi, Achronix, QuickLogic, Gowin offer RISC-V CPUs for their FPGAs
- These vendors provide an alternative to open-source CPUs
  - Fully validated, manufacturable, supported cores for customers willing to pay

RISC-V Ecosystem Expands Rapidly



- Other IP vendors offer related IP for RISC-V
  - Rambus security core, Tortuga security framework, UltraSoC debug, Hex Five TEE
- Many commercial vendors adding RISC-V support to design tools
  - E.g. AntMicro (simulator), Imperas (emulator), VectorBlox (perf analysis)
- Both new and established vendors offer design services for RISC-V SoCs
- Open-source tools available for software development
- Several versions of Linux available (Fedora, Debian, Yocto, FreeBSD...)
- Many universities working on open-source projects
  - Including CPUs, other IP, design tools, and software

Roadmap to Higher Performance

- Current cores mainly target microcontroller designs
- SiFive 7 series is fastest licensible RISC-V CPU
  - Dual-issue in-order 8-stage pipeline
  - Optional FPU, optional MMU, 32-bit or 64-bit
- Esperanto developing high-performance “Maxion” RISC-V CPU
  - 64-bit out-of-order core aims to beat performance of Cortex-A76
  - Esperanto will use Maxion in its AI processor and also license the design
- DSP and vector extensions in development
  - Several vendors have already added extensions to boost AI and signal processing
  - RISC-V will standardize these extensions to simplify design, compatibility

Roadmap to Greater Shipments

- Huami ships ~20 million wearable devices per year
- Nvidia ships ~40 million GPUs per year
- Western Digital to convert >1 billion cores to RISC-V by 2020
  - Mostly microcontrollers for flash-memory sticks (replaces ARC)
  - May use SiFive, Esperanto cores for large storage systems
- If Qualcomm adopts RISC-V for embedded core (e.g. PMIC), it could appear in ~800 million Snapdragon chips per year
- Vendors targeting IoT are selling into ~2 billion unit market (2022)
  - Most IoT devices use ARM MCU today

Roadmap to Larger Ecosystem

- Need Google to port Android for access to many consumer devices
- Need commercial RTOS support (e.g. Green Hills, Nucleus, QNX)
  - RISC-V currently restricted to FreeRTOS and open-source Zephyr
- Need support from top foundries to certify RISC-V IP suppliers
- Need driver support from top-tier IP vendors
  - Simplify connecting GPU, memory, I/O to RISC-V CPU
- Open-source efforts good for universities and startups, but large customers want commercial support

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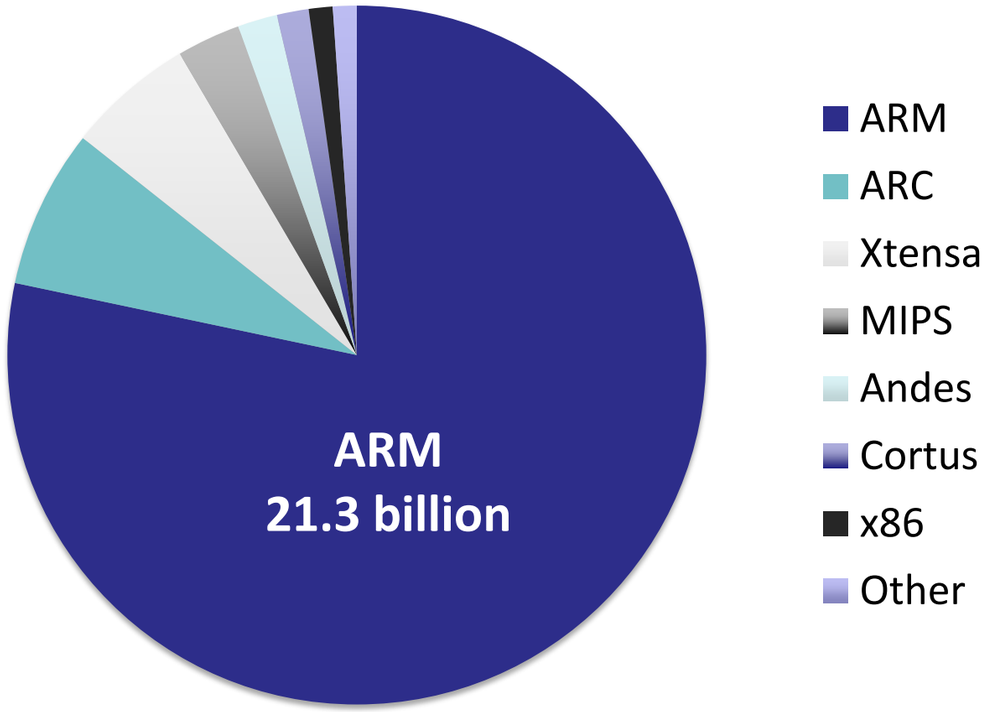
Most Popular Instruction Sets

Chip Shipments by Instruction Set, 2017



Chips using 32/64-bit CPUs; may include double counting
(Source: vendors, The Linley Group estimates)

- ARM is by far the most popular instruction set today by units
- Synopsys (ARC), Cadence (Xtensa), Wave (MIPS) are top competitors by unit shipments
- RISC-V chips have yet to ship in significant volume
- Most ARM volume comes from microcontrollers (MCUs) for automotive, IoT, and embedded

RISC-V Strengths

Professor David Patterson

- No ISA license fee—good for universities, startups
  - For larger vendors, CPU license fee is a small part of design cost
- Open-source cores available with no license fees
- Commercial cores available from several vendors
  - Only ISA with multiple sources
  - Lower license fees than ARM
- Users can add custom instructions
  - ARM doesn't permit customers to change ISA, even with architecture license
  - Andes offers tools (e.g. COPILOT) to assist customers with adding instructions

Commercial RISC-V Core Beats ARM in PPA

- Customers seek better performance, power, and die area
- Andes N25 uses much less area and power than similar Cortex-M33
  - Both cores are simple scalar microcontrollers with optional FPU (not shown)
  - Both support 16/32-bit instructions
  - Both include debug, interrupt logic

	ISA	Max Speed	CM/MHz	µW/MHz	Die Area
Andes N25	32-bit RISC-V	1,000MHz	3.58 CM	4.1µW	0.033mm^2
Cortex-M33	32-bit ARMv8	675MHz*	3.86 CM	9.0µW*	0.050mm^2
RISC-V Advantage		**1.5x**	**0.93x**	**2x**	**1.5x**

All data for 28HPC+, base configuration excluding memory

(Source: vendors except *The Linley Group estimate)

ARM Strengths

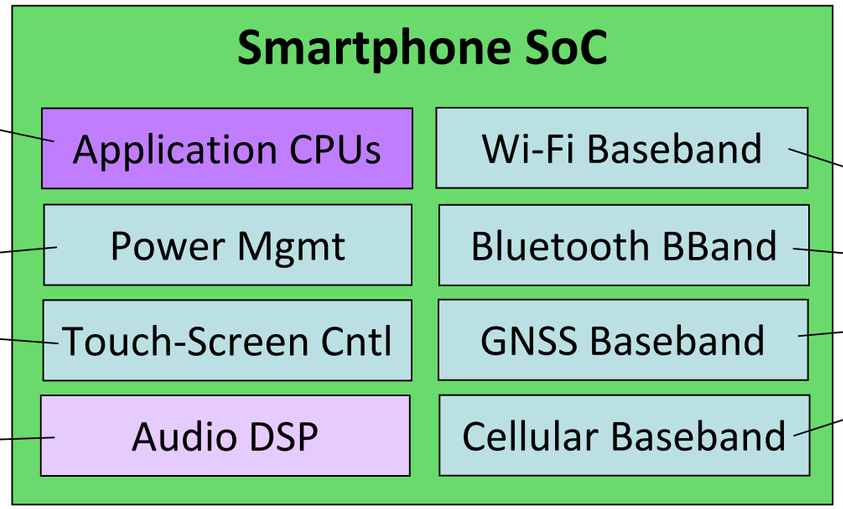
- Broad range of cores with well-funded roadmap
  - Big portfolio good for chip vendors with many projects
  - RISC-V good for individual designs
- Strict software compatibility simplifies software distribution
  - Most important for markets with much third-party software (e.g. smartphone AP)
  - RISC-V good for embedded applications or embedded cores in SoC
- Vast ecosystem provides many options for SoC designers
  - ARM cores certified with all major foundries, all major IP vendors, and software
  - RISC-V is still young; ecosystem continues to grow

Opportunities in Mobile for RISC-V

Runs 3rd party apps
HARD FOR RISC-V

Small MCU cores embedded in SoC
GOOD FOR RISC-V

Needs DSP extensions
POSSIBLE FOR RISC-V



Each of these units has a small MCU core to implement high-level protocol and control functions
GOOD FOR RISC-V

- Mobile SoC has many embedded cores besides application CPUs
  - RISC-V is a good fit for wireless baseband, power management, touch-screen controller
  - With DSP extensions, could also handle audio

Conclusions

- RISC-V shipments are small today, but momentum is building
- Open-source cores are useful but lack commercial features, support
- Licensed RISC-V cores are fully qualified for commercial designs
- Some RISC-V cores already offer better PPA than ARM
- Current RISC-V cores well suited to embedded, automotive, and IoT
- Can also serve as embedded cores in mobile, PC, and server processors
- Roadmap includes higher-performance cores in 2019
- With many companies participating, RISC-V ecosystem will keep growing

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